Sub E1

1. (Twice Amended) An apparatus for [generating an] disabling a masked interrupt wherein an [, said] interrupt is being requested by an assertion of an interrupt request signal, said apparatus comprising:

D1

means for indicating a software condition;

means for indicating a hardware condition; and

means for unmasking [generating] said masked interrupt in response to the assertion of said interrupt request signal and at least one of [, said means for generating responsive to] said indicated software condition and said indicated hardware condition.

Sub E2

3. (Amended) An apparatus as recited in claim [2] 1 wherein said means for [generating] unmasking comprises:

D2

means for enabling [said interrupt] an unmasking circuit in response to at least one of said indicated software condition and said indicated hardware condition; and

means for asserting said interrupt when said interrupt request signal is asserted and said [interrupt] unmasking circuit is enabled and for not asserting said interrupt when said interrupt request signal is asserted and said [interrupt] masking circuit is not enabled.

In claim 4, line 1, change "3" to --1--.

In claim 5, line 1, change "4" to --1--.

Sub E4

6. (Amended) An apparatus as recited in claim [5] 3 wherein said means for enabling said [interrupt] unmasking circuit comprises an OR gate that receives [said] at least one of an indicated software condition enable signal and [said] an indicated hardware condition enable signal and that outputs a combined enable signal.

D3

In claim 7, line 1, change "6" to --27--.

Sub E7

23. (Amended) In a processor that may enter a [certain] predetermined state from which it may only escape via an interrupt, and wherein while said processor is in said predetermined state all interrupts are masked [in which certain state all interrupts may be masked, and further in which certain state no interrupt may be unmasked conventionally], a circuit for unmasking [overriding] a masked interrupt, said circuit comprising:

D4

a first subcircuit that receives a first signal for indicating whether said processor is in said predetermined state and at least one of an external signal and a software enable signal, said first subcircuit produces an unmasking signal based on whether said first signal indicates that said processor is in said predetermined state and whether at least one of said software

enable signal and said external signal request an interrupt to be masked;

a second subcircuit that receives said unmasking signal and a first interrupt request signal, said second subcircuit produces a second interrupt request signal based on said unmasking signal and said first interrupt signal; and

a third subcircuit responsive to said interrupt signal for interrupting said processor

[a first subcircuit that provides a first signal to enable conventional unmasking, which first signal would be ineffective alone to effect unmasking when said processor is in said certain state;

a second subcircuit that provides a second signal that indicates that said processor is in said certain state; and

a third subcircuit, responsive to said first signal and said second signal, and further responsive to an interrupt request signal, for generating an interrupt request].

24. (Amended) A circuit as recited in claim 23, wherein said [certain] predetermined state is an idle state.

25. (Amended) A circuit as recited in claim 23, wherein said [third] second subcircuit comprises an AND gate.

Please add the following claims:

27. An apparatus for generating an interrupt, said interrupt being requested by an assertion of an interrupt request signal, said apparatus comprising:

means for indicating a software condition comprising a programmable register that outputs a software enable signal;

means for indicating a hardware condition that comprises at least one hardware circuit, and wherein each of said at least one hardware circuit outputs a hardware enable signal; and

means for generating said interrupt in response to the assertion of said interrupt request signal and at least one of said indicated software condition and said indicated hardware condition, said means for generating comprises:

means for enabling said interrupt in response to said software condition and said hardware condition, said means for enabling said interrupt comprises an OR gate that receives said software enable signal and said hardware enable signal and that outputs a combined enable signal; and

means for asserting said interrupt when said interrupt request is asserted and said interrupt is enabled and for not asserting said interrupt when said interrupt request is asserted and said interrupt is not enabled.

28. An apparatus as recited in claim 3, wherein said means for asserting comprises an AND gate that receives said combined enable signal and said interrupt request signal and that outputs said interrupt.

29. An apparatus as recited in claim 5, wherein said apparatus is included in a processor, and wherein said at least one hardware circuit asserts said hardware enable signal in response to an external enable signal generated external to said processor.

30. An apparatus as recited in claim 5, wherein said apparatus is included in a processor, and wherein said at least one hardware circuit asserts said hardware enable signal when said processor is in a particular state.

31. An apparatus as recited in claim 30, wherein said particular state comprises an idle mode.

32. An apparatus as recited in claim 30, wherein said at least one hardware circuit further generates said hardware enable signal in response to an external enable signal generated external to said processor.